GURU NANAK DEV ENGINEERING COLLEGE
BIDAR -585403

Affiliated to Visvesvaraya Technological University, Belagavi
Approved by AICTE, New Delhi & Accredited by NAAC with A++ Grade

2022 SCHEME

BASIC ELECTRONICS
(BBEE103/203)

[As per Choice Based Credit System (CBCS)]

(Strictly for internal circulation only)

MODULE- 2

Name of the staff I/C: **Prof. Ramesh Patil,**
E&CE Department

Module – 2

Bipolar Junction Transistors: Introduction, BJT Voltages & Currents, BJT Amplification, Common Base Characteristics, Common Emitter Characteristics, Common Collector Characteristics, BJT Biasing: Introduction, DC Load line and Bias point (Text 1: 4.2, 4.3, 4.5,4.6, 5.1)

Field Effect Transistor: Junction Field Effect Transistor, JFET Characteristics, MOSFETs: Enhancement MOSFETs, Depletion Enhancement MOSFETs (Text 1: 9.1,9.2,9.5)

Text Books :

1. Electronic Devices and Circuits, David A Bell, 5th Edition, Oxford, 2016

Prof. RAMESH PATIL
E&CE Dept.
GNDEC, Bidar.

Module-2

* Bipolar Junction Transistor (BJT)

When a third doped element is added to diode in such a way that two pn junctions are formed. The resulting device is known as a transistor.

A junction transistor is simply a sandwich of one type of semiconductor material (p-type or n-type) between two layers of the opposite type. Accordingly there are two types of transistors.

i) npn transistor
ii) pnp transistor.

An npn transistor is composed of two n-type semiconductors seperated by a thin section of p-type as shown in fig.

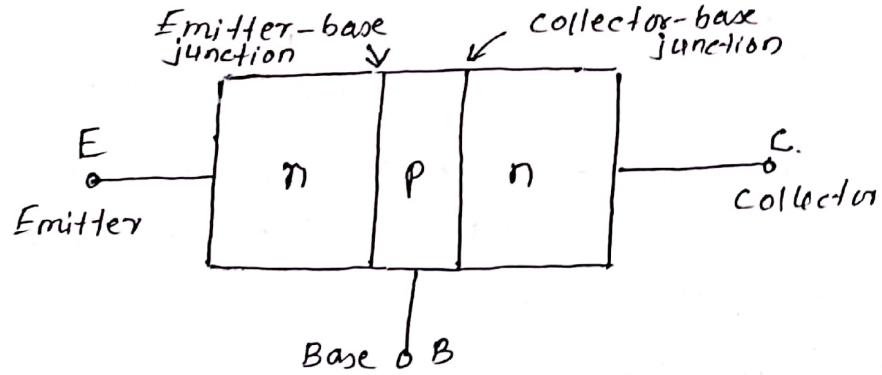


fig. npn transistor.

The centre layer is called the base, one of the outer layers is termed the emitter, and the other outer layer is referred to as the collector. The emitter, base, and collector are provided with terminals which are appropriately labelled E, B and C.

A pnp transistor is formed by two p-sections seperated by a thin section of n-type semiconductor as shown in fig.

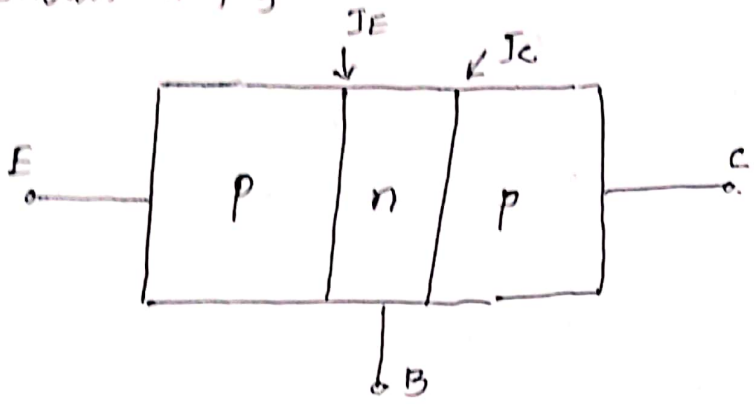
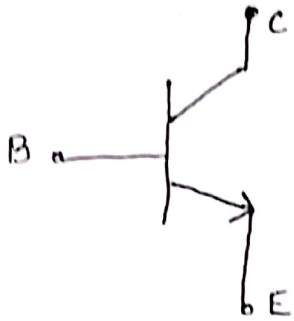
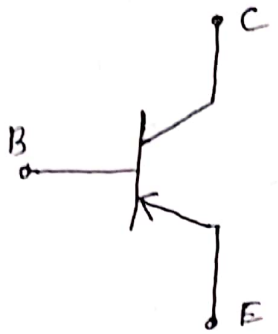


fig. pnp transistor.

Circuit symbols for npn and pnp transistors are shown in fig.



npn transistor.



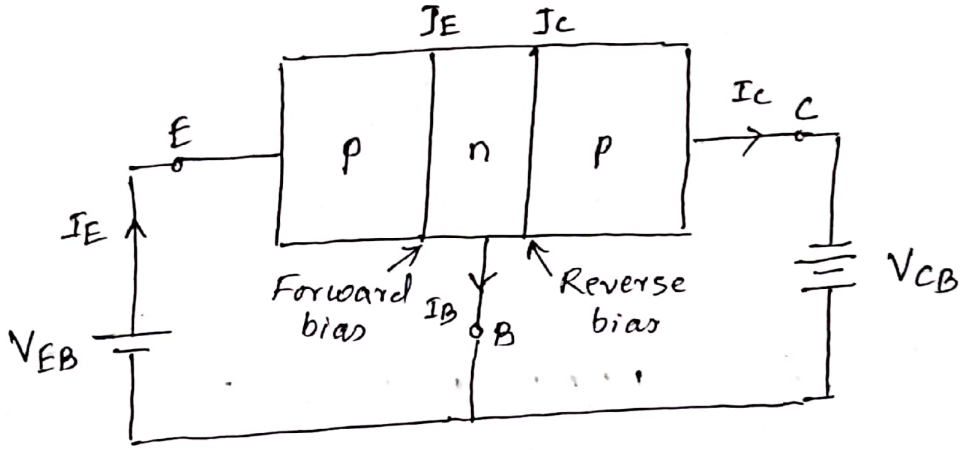
pnp transistor.

The arrowhead on each symbol identifies the transistor emitter terminal, and indicates the conventional direction of current flow.

- transistor terminals.

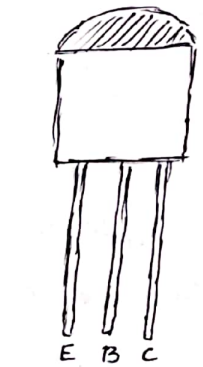
i) Emitter: The section on one side that supplies charge carriers (electrons or holes) is called emitter. The emitter is always forward biased with respect to base so that it can supply a large number of majority carriers.

ii) Collector: The section on the otherside that collects the charges is called the collector. The collector is always reverse biased. Its function is to remove charges from its junction with the base.

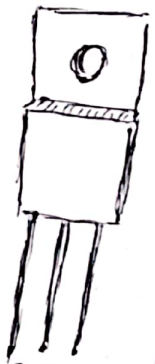


iii) Base : The middle section which forms two p-n junction between the emitter and collector is called base. The base - emitter junction is forward biased, allowing low resistance for the emitter circuit. The base- collector junction is reverse biased and provides high resistance in the collector circuit.

Two transistor packages are illustrated in fig, a Low power transistor and a high power device.



Low power transistor

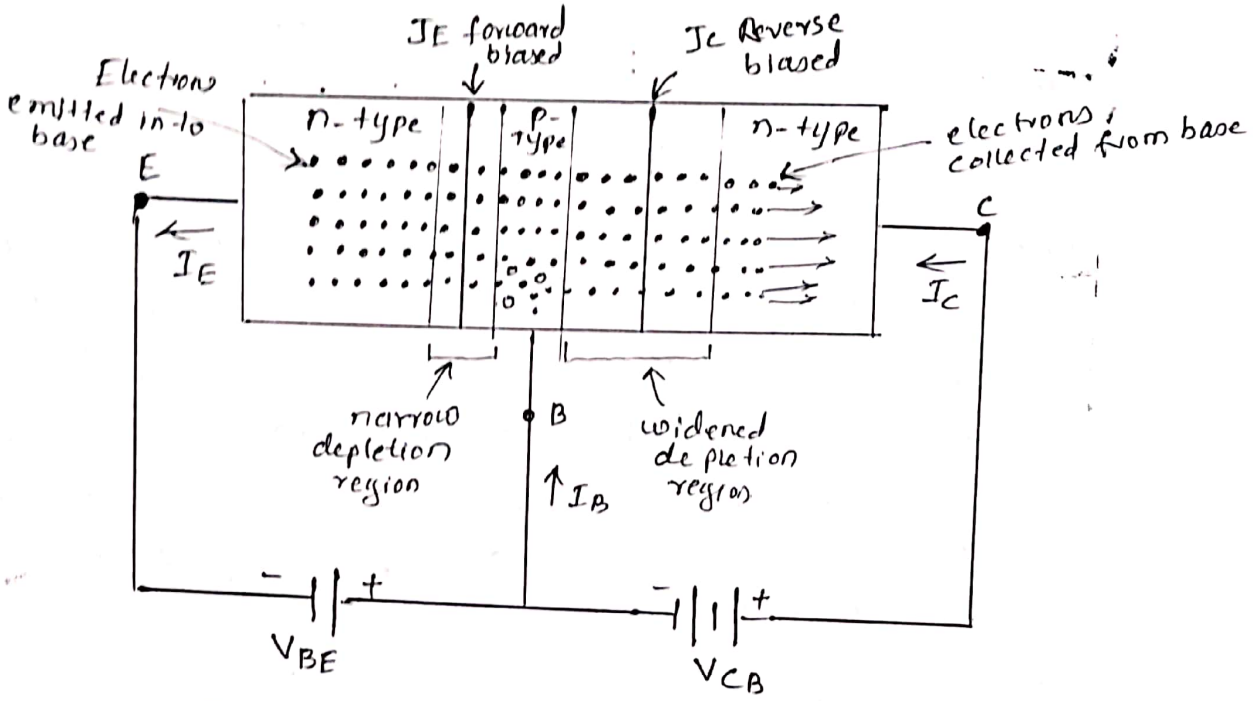


High power transistor.

A low power transistors typically pass currents of 1 mA to 20 mA. Current levels for high power transistors range from 100 mA to several amps.

* npn Transistor operation

Consider the fig. shown below which shown an npn transistor with external bias voltages.



For normal operation, the emitter-base (J_E) junction is forward biased and collector-base (J_C) junction is reverse biased. The forward bias causes the electrons in the n-type emitter to flow towards the base. This constitutes emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes. As the base is lightly doped and very thin, therefore only a few electrons (less than 2%) combine with holes to constitute base current I_B. The remaining electrons (more than 98%) cross over into the collector region to constitute collector current I_C. In this way almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base current.

i.e $I_E = I_B + I_C$

pnp transistor operation is same as an npn transistor, with the exception that majority charge carriers are holes. The polarities of voltages are in a such a way that emitter-base junction is forward biased and collector-base junction is reverse biased.

* BJT Voltages and Currents.

* Terminal voltages.

The terminal voltage polarities for an npn transistor are shown fig.a).

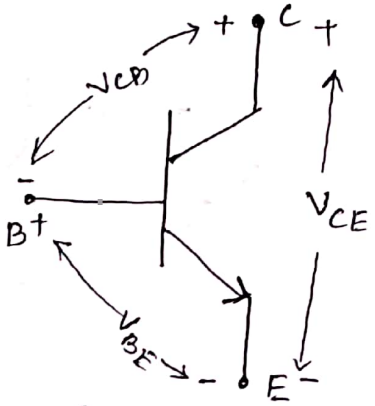


fig.a: npn terminal voltage polarities.

The direction of arrowhead indicates conventional current direction and also the transistor bias polarities. For npn transistor, the base is biased positive with respect to emitter, and the arrowhead points from the base to emitter. The collector is then biased to higher positive voltage than the base.

Fig. b) shows that the voltage sources are usually connected to the transistors via resistors.

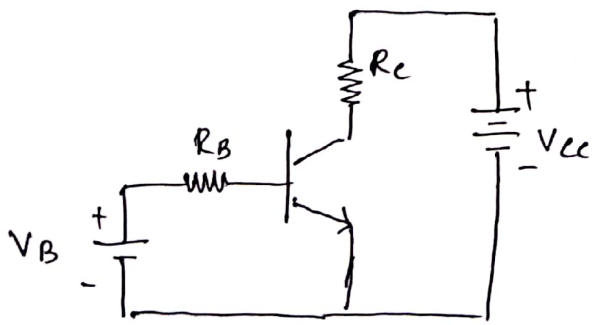
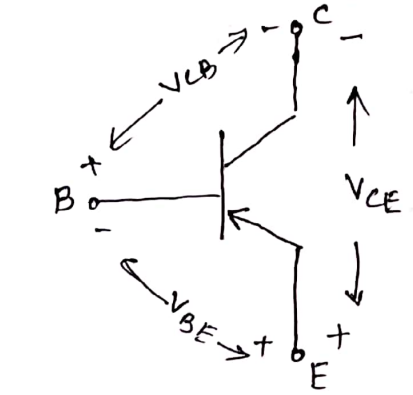


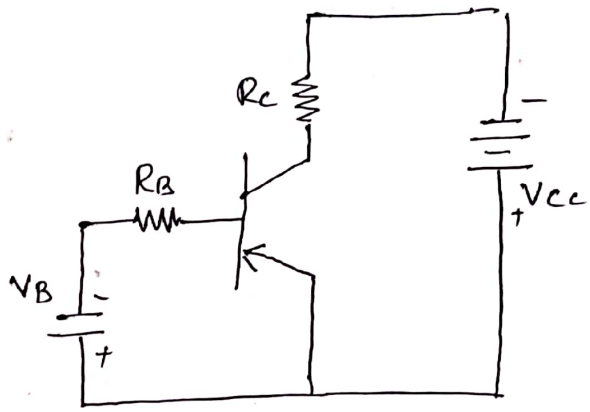
fig b. voltage source connections.

The base bias voltage V_B is connected via resistor R_B and collector supply V_{cc} is connected via resistor R_C. The negative terminals of the two voltage sources are connected at the transistor emitter terminal.. V_{cc} is always much larger than V_B. and this ensures that the CB junction remains reverse biased.

The terminal voltage polarities for a pnp are shown in fig.



pnp terminal voltage polarities.

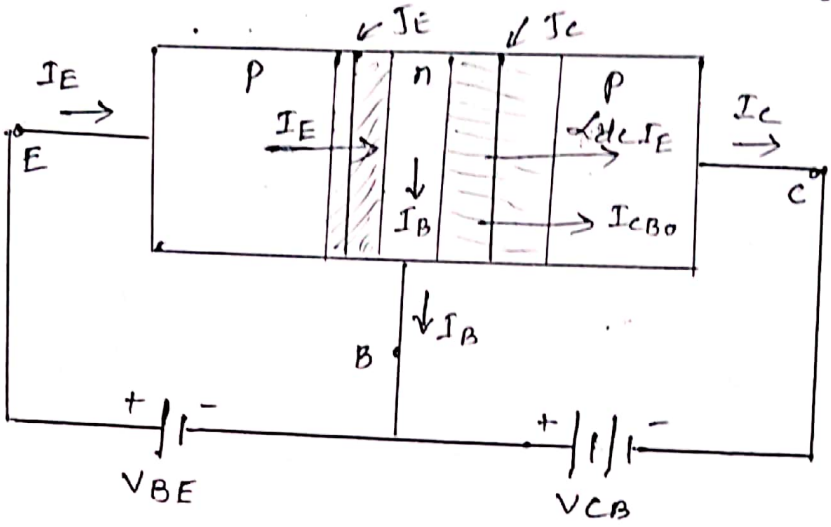


Voltage source connections.

All transistors (npn and pnp) are normally operated with CB junction reverse biased and BE junction forward biased.

* Transistor Currents

The various current components that flow within a transistor are illustrated in fig. shown.



The current flowing into the emitter terminal is referred to as the emitter current and is identified as I_E. The emitter current I_E consists of hole current (holes crossing from emitter into the base) and electron current (electrons crossing from base into the emitter).

Base current I_B and collector current I_C are also shown as conventional current direction. Both I_B and I_C flow out of the transistor, while I_E flows into the transistor

$$\therefore I_E = I_C + I_B \quad \text{— 1)}$$

As already discussed, almost all of I_E crosses into the collector and only a small portion flows out of the base terminal. Typically 96% to 99.5% of I_E flows across the collector-base junction to become the collector current.

$$\therefore I_C = \alpha_{dc} I_E \quad \text{— 2)}$$

α_{dc} is the emitter-to-collector current gain, or the ratio of collector current to emitter current.

$$\therefore \alpha_{dc} = \frac{I_C}{I_E} \quad \text{— 3)}$$

α_{dc} is also termed as the common-base dc current gain. Because the CB junction is reverse biased, a very small reverse saturation current (I_{CBO}) flow across the Jc junction. I_{CBO} is named the collector-to-base leakage current and is normally so small that it can be neglected.

Substituting for I_E from eqn 1) into to eqn 2) we get

$$I_C = \alpha_{dc}(I_C + I_B)$$

$$\Rightarrow I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} \cdot I_B$$

above eqn can be rewritten as

$$I_C = \beta_{dc} \cdot I_B \Rightarrow \beta_{dc} = \frac{I_C}{I_B} \quad \text{— 4)}$$

where $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$ — 5)

β_{dc} is the base to collector current gain. or the ratio of collector current to Base current.

- Relationship between α and β.

W.KT $I_E = I_C + I_B$

dividing LHS & RHS by I_C

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta+1}{\beta} \Rightarrow \alpha = \frac{\beta}{1+\beta} \quad \text{— 6)}$$

Ex: Calculate I_C & I_E for a transistor that has $\alpha_{dc} = 0.98$, $I_B = 100\,\mu A$. Also determine the value of β_{dc} for the transistor.

Soln:

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.98}{1-0.98} = 49$$

$$I_C = \beta_{dc} \cdot I_B = 49 \times 100 \times 10^{-6} = 4.9\,mA$$

$$I_E = I_C + I_B = 4.9 \times 10^{-3} + 100 \times 10^{-6}$$
$$= 4.9\,mA + 0.1\,mA$$
$$= 5\,mA.$$

Ex: Calculate α_{dc} and β_{dc} for the transistor shown in fig. if I_C is measured as 1mA and I_B is $25\,\mu A$. Also determine the new base current to give $I_C = 5mA$.

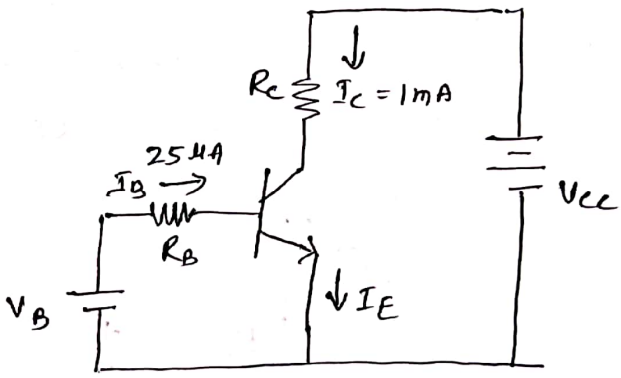
Soln:

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{1 \times 10^{-3}}{25 \times 10^{-6}}$$
$$= 40$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{40}{41}$$
$$= 0.976$$

when $I_C = 5mA$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{5 \times 10^{-3}}{40} = 125\,\mu A.$$



Ex:

* BJT Amplication.

An amplifier is a circuit, which can be used to increase the amplitude of the input voltage or current at the output. Amplifiers are used in music equipment, electronic devices such as television and radio receivers, audio equipment etc.

* Current amplification.

We know that, the equations.

$$\alpha_{dc} = \frac{I_C}{I_E} \quad \text{and} \quad \beta_{dc} = \frac{I_C}{I_B}$$

demonstrate that a transistor can be used for current amplification. A small change in the base current ΔI_B produces a large change in collector current ΔI_C and large emitter current change ΔI_E. See fig a) and b).

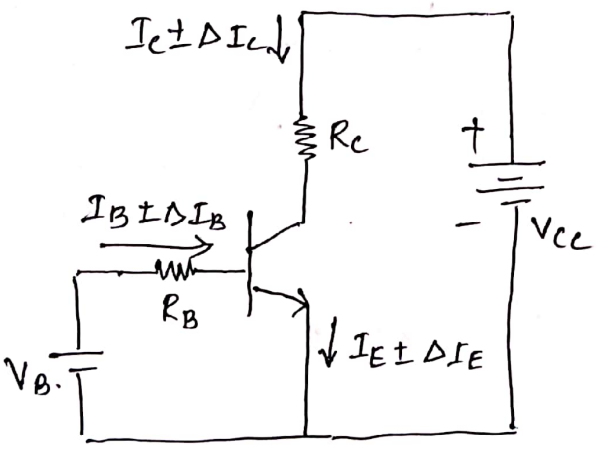


fig. a)

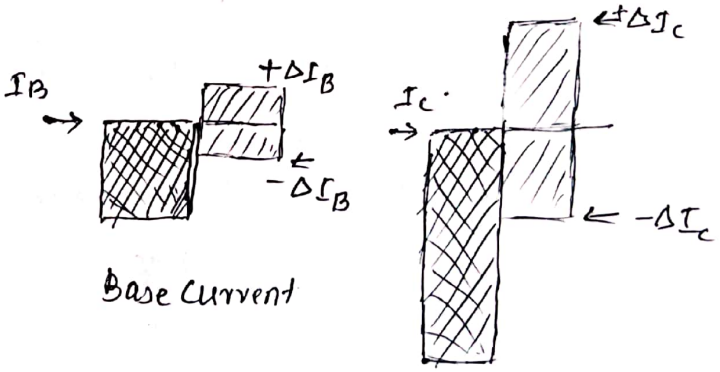


fig. b.

Rewriting the eqn β_{dc}, the current gain from the base to collector can be stated in terms of current level changes

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

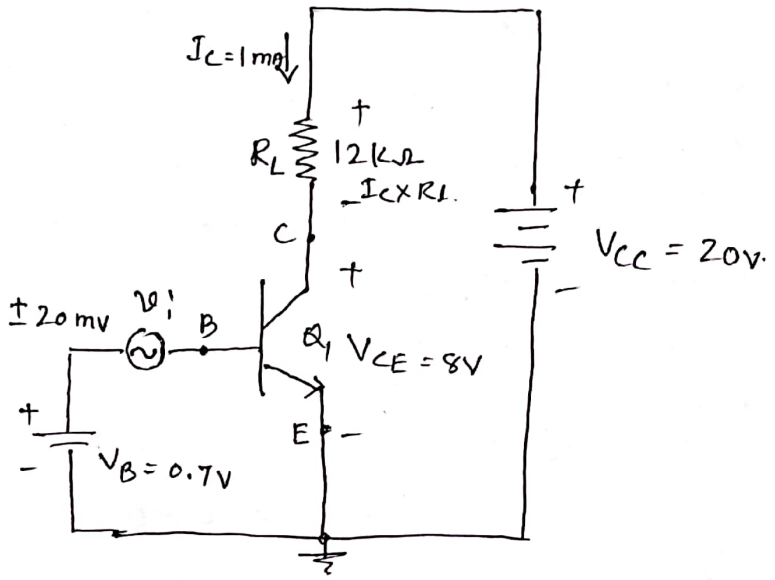
Changing currents are called alternating quantities (a.c).

$$\beta_{ac} = \frac{I_c}{I_b}.$$

* Typical value of β_{dc} ranges from 25 to 300.

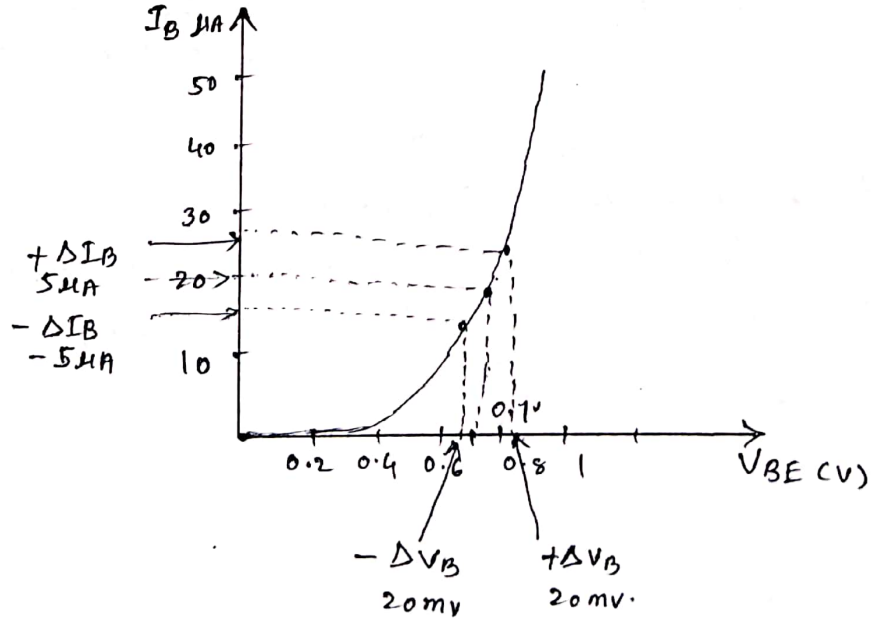
* Voltage Amplification.

Consider a transistor circuit in CE configuration as shown in fig.



Assume that the transistor Q_1 has $\beta_{dc} = 50$ Note that 0.7v dc voltage source V_B forward biases the transistor base-emitter junction. An ac signal source v_i in series with V_B provides a ±20mv input voltage.

If Q_1 has the I_B V/s V_{BE} characteristics as shown in fig. The 0.7v level of V_B produces a 20μA base current.



This gives $I_C = \beta_{dc} I_B = 50 \times 20 \times 10^{-6}$

$= 1 \times 10^{-3} = 1\,mA.$

$V_{CE} = V_{cc} - I_C R_L = 20 - 1 \times 10^{-3} \times 12 \times 10^{3}$

$= 8V.$

When ac input v_i is Zero, the transistor V_{CE} remains at 8V. When v_i causes a base voltage variation (ΔV_B) of $\pm$ 20 mv, the base current changes by $\pm$ 5 μA as shown in graph.

The I_B change produces a collector voltage change.

$\Delta I_C = \beta_{dc} \times \Delta I_B = 50(\pm 5 \times 10^{-6})$

$= \pm 250\,\mu A$

$\Delta V_{CE} = \Delta I_C R_L = \pm 250 \times 10^{-6} \times 12 \times 10^{3}$

$= \pm 3V$

The circuit ac input is the base voltage change ΔV_B and the ac output change is the collector voltage ΔV_{CE}. Because the output is greater than the input, the circuit has a voltage gain. So it is a voltage amplifier. The voltage gain A_v is the ratio of output voltage to input voltage.

$\therefore A_v = \frac{\Delta V_{CE}}{\Delta V_B} = \frac{\pm 3V}{\pm 20\,mV} = \frac{3}{20 \times 10^{-3}}$

$= 150$

Therefore, the ac signal voltage v_i produces the ac base current I_b and this generates the ac collector current I_c, which produces the ac voltage change across R_L

* Transistor configurations.

There are three leads in a transistor emitter, base and collector terminals. But, when a transistor is connected in a circuit, 4 terminals are needed, 2 for input and 2 for output. This difficulty is overcome by making one of the terminals common to both input and output terminals. So transistor can be connected in a circuit in 3 ways.

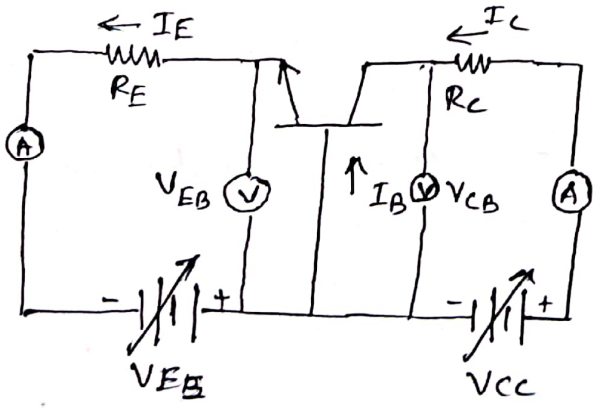
1) Common - Base Configuration (CB)
2) Common - Emitter configuration (CE)
3) Common - Collector configuration (CC)

To understand complete electrical behavior of a transistor it is necessary to study the interrelation of various currents and voltages of transistor. These relationships can be plotted graphically which are commonly known as the characteristics of transistor. The most important characteristics of transistor in any configuration are input and output characteristics.

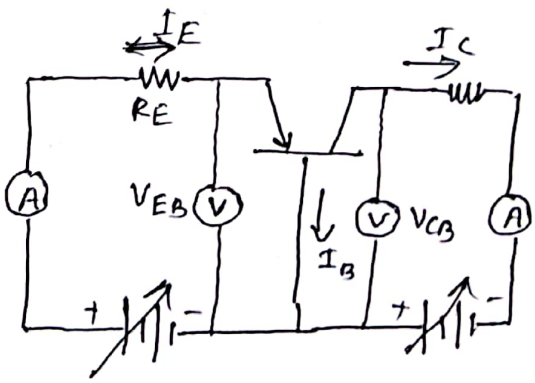
* Common - Base Characteristics.

Common - Base Circuit (CB Confn)

Fig shows the common-base configuration or Connection.



for npn transistor

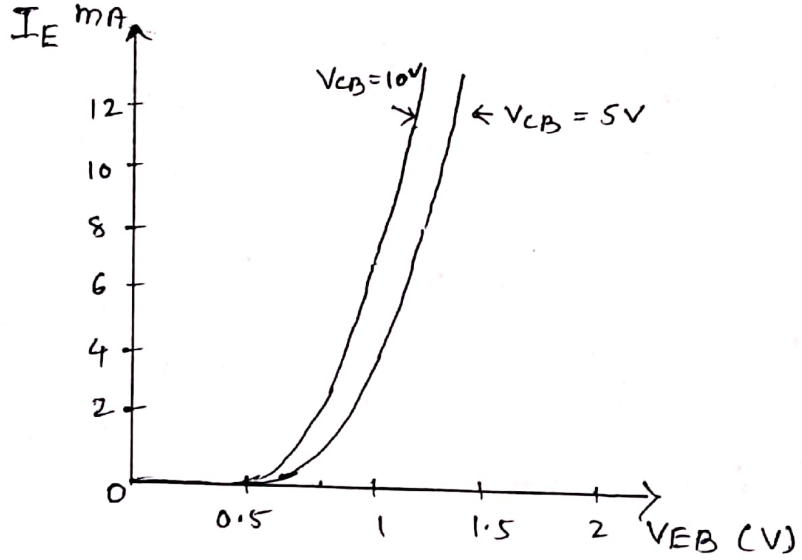


for pnp transistor.

In this configuration input is applied between emitter and base and output is taken from the collector and base. Here base of the transistor is common to both input and output circuits and hence the name common-base configuration.

- Input characteristics.

It is the curve between input current I_E and input voltage V_{EB} at constant collector-base voltage V_{CB}. (graph of I_E V/s V_{EB} at constant V_{CB}) as shown in fig.



To determine the input characteristics, the output voltage V_{CB} is maintained constant and input voltage V_{EB} is set at several convenient levels. For each level of input voltage, the input current I_E is recorded. I_E is then plotted versus V_{EB} to give common-base input characteristics.

Because the EB junction is forward biased, the common-base input characteristics are essentially those of forward biased pn-junction.

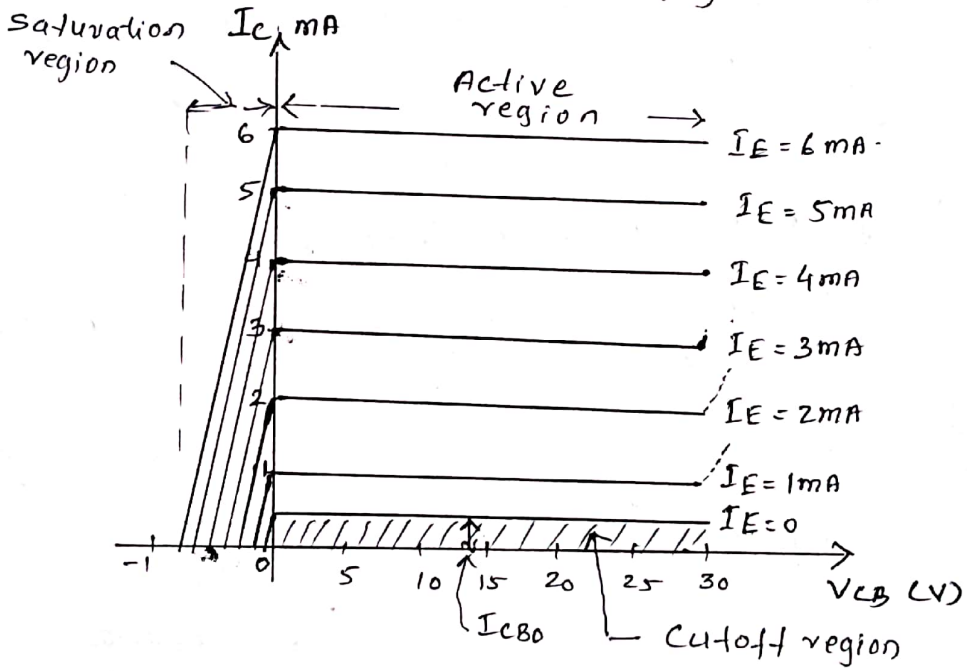
It can be observed that there is slight increase in emitter current I_E with increase in V_{CB}. This is due to change in the width of the depletion region

in the base region under reverse biased condition. Due to this the electrical base width is reduced. This effect is called as 'Early effect'. Because of this effect there will be reduction in the base width which increases charge concentration. This causes more diffusion of electrons n-type emitter to p-type base increasing emitter current slightly.

- Output Characteristics.

It is the curve between collector current I_C and collector base voltage V_{CB} at constant emitter current I_E. (Graph of I_C V/s V_{CB} at constant I_E).

Fig. shows the output characteristics of a typical transistor in common-base configuration.



from the characteristics we observe the following points

1) The output characteristics has three basic regions Active, cutoff and saturation regions.
2) For the operation in the active region, the emitter base junction is forward biased while collector base junction is reverse biased. In this region Collector current is I_C is approximately equal to the emitter current I_E.

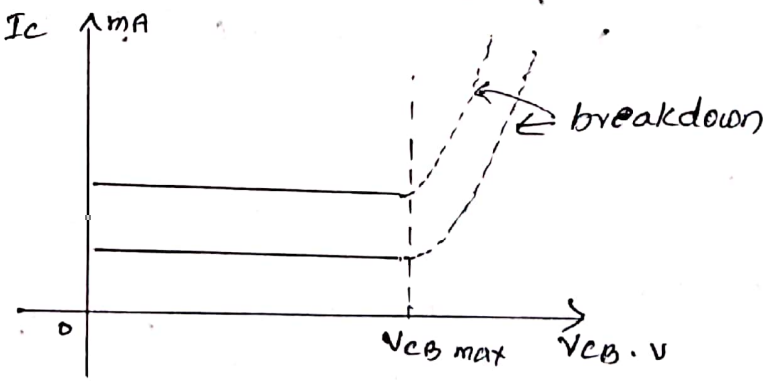
3) If the emitter current is zero, the collector current I_C is simply I_{CBO} as shown in o/p characteristics.

4) Saturation region is that region of the characteristics which is left of $V_{CB} = 0$. When V_{CB} is reduced to zero, I_C still flows. Even when V_{CB} is zero, there is still barrier voltage existing at the CB junction and this assists the flow of I_C. To stop the flow of carriers, the CB junction has to be forward biased. In the saturation region both the junctions are forward biased.

5) The region below $I_E = 0$ is cutoff region, where $I_C = I_{CBO}$. In this region both the junctions are reverse biased.

* punch through effect:

If the reverse bias voltage on the CB junction is allowed to exceed the maximum safe limit specified by the manufacturer, device breakdown may occur. as shown in fig.

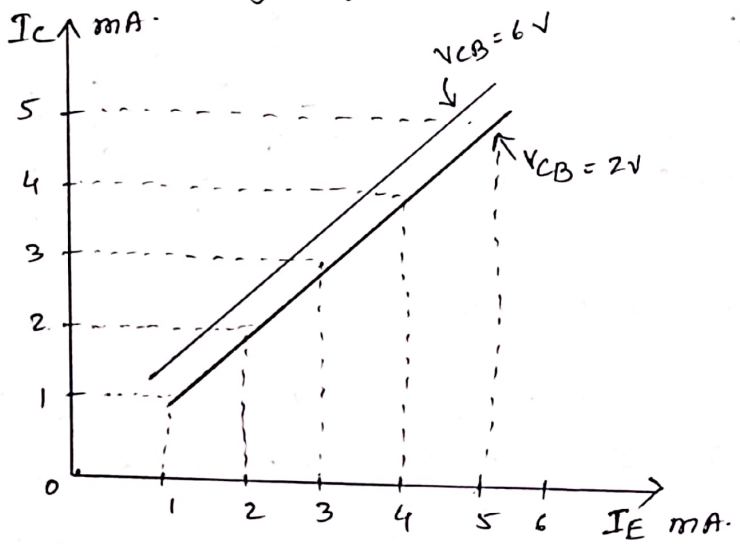


Breakdown may be caused by the same effects that make diode breakdown. Breakdown can also result from the CB depletion region penetrating in to the base until it makes contact with the EB depletion region. this condition is known as 'punch-through effect'

* Current gain characteristics (CB confn).

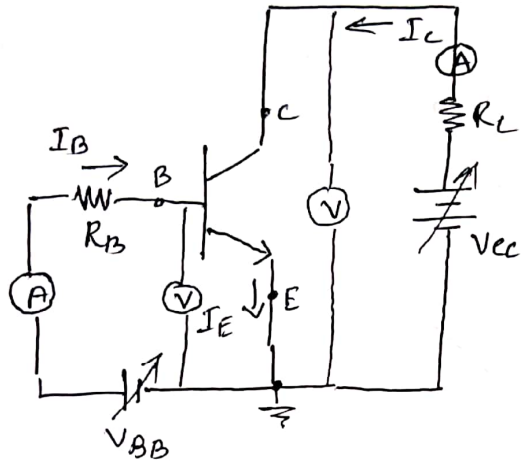
The current gain characteristics are a graph of output current I_C versus input current I_E at constant V_{CB}.

For plotting these characteristics V_{CB} is kept fixed at a convenient level and I_C levels are measured for various settings of I_E.

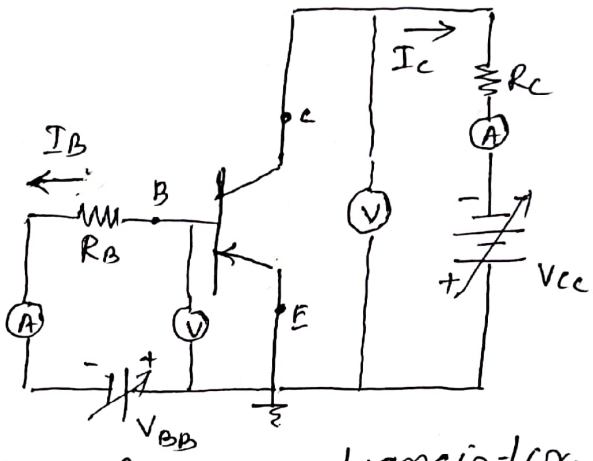


* Common-Emitter Characteristics (CE confn)

Fig shows the common-emitter configuration.



for npn transistor

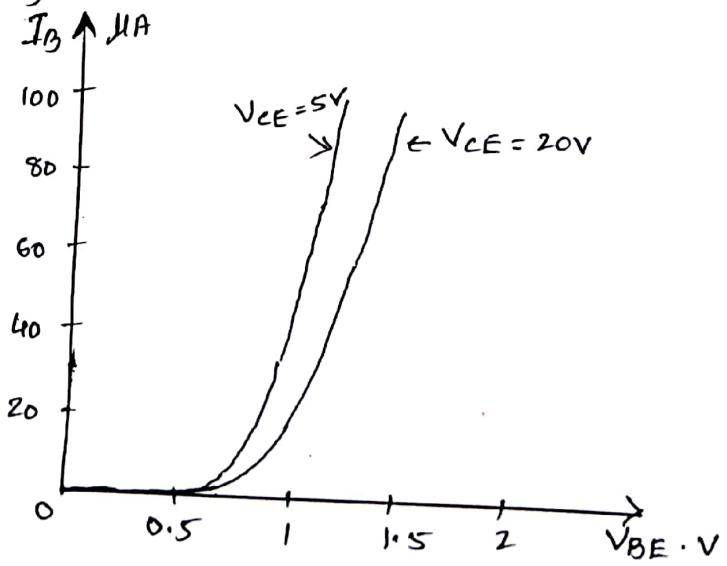


for pnp transistor.

The input is applied between the Base and Emitter terminals, and the output voltage is taken at the Collector and emitter terminals. Here, emitter of the transistor is common to both input and output Circuits and hence the name common-emitter configuration.

* Input Characteristics.

It is the curve between input base current I_B and input voltage V_{BE} at constant collector-emitter voltage V_{CE}. (graph of I_B V/s V_{BE} at constant V_{CE}). as shown in fig.

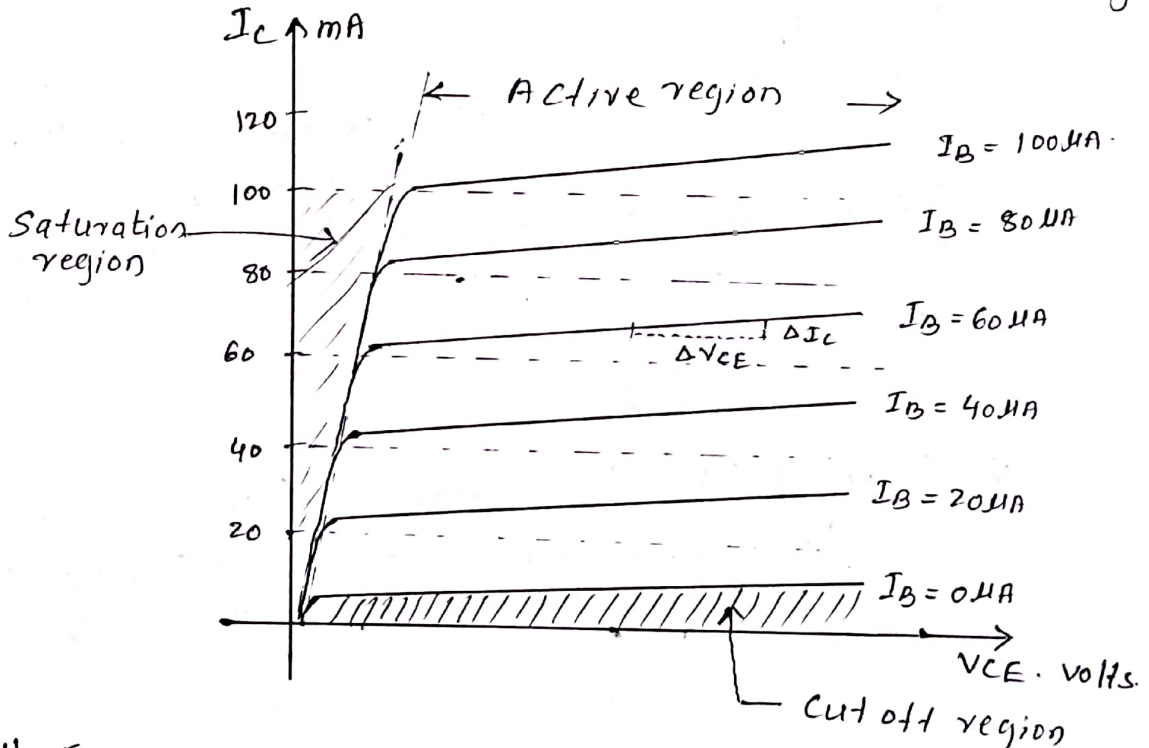


1) It is seen that input characteristics are those of a forward-biased pn junction. After the cut-in voltage the base current increases rapidly with small increase in V_{BE}. It means that dynamic input resistance is small in CE configuration

2) For fixed value of V_{BE}, I_B decreases as V_{CE} is increased because of fewer recombinations.

* Output Characteristics (CE conf?)

This characteristics shows the relation between the collector current I_C and collector voltage V_{CE}, at various fixed values of I_B. It is graph of I_C V/s V_{CE} at constant I_B. as shown in fig



1) From the characteristics we can see that change in ΔV_{CE} causes little change in the collector current ΔI_C. for constant base current. Hence output dynamic resistance is high in CE conf?

2) The output characteristics of CE configuration consists of three regions: Active, saturation and cut off regions.

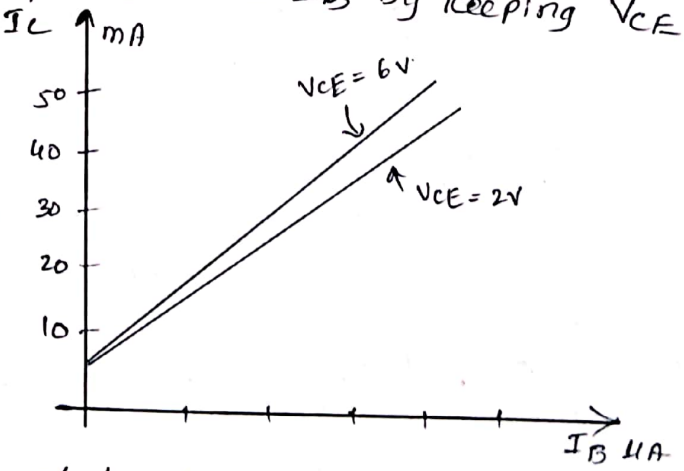
3) Active region: The region where the curves are approximately horizontal is the active region of CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased depletion region spread more in base reducing the chances of recombination. This increases the value of α_{dc}. This early effect causes collector current to rise more sharply with increasing V_{CE}.

4) Saturation region: If V_{CE} is reduced to a small value such as 0.2 V, then collector-base junction becomes forward biased. Since the emitter-base junction is already forward biased by 0.7 V. When both junctions are forward biased, the transistor operates in saturation region, which is indicated on output characteristics.

5) Cutoff region: When the base input current made equal to zero, the collector current is the reverse Lakage current I_{CEO}. The region below $I_B = 0$ is the cutoff region of operation for transistor In this region both the junctions of the transistor are reverse biased.

* Current gain characteristics (Transfer characteristics)

Transfer characteristics in CE configuration is the graph of I_c versus I_B by keeping V_{CE} constant

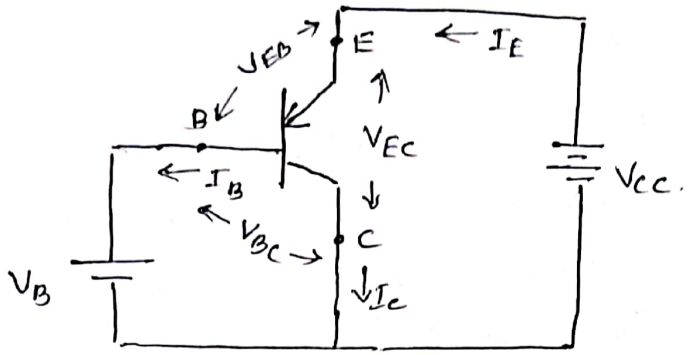


Current gain of transistor in CE conf. is given as

$$\beta = \frac{I_c}{I_B}$$

* Common - Collector Configuration

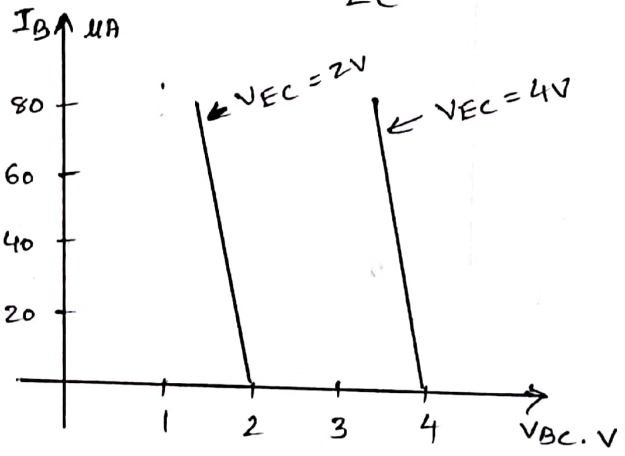
Fig. shows the common collector configuration.



In this configuration input is applied between base and collector, and output is taken from emitter and collector. Here, collector of the transistor is common to both input and output circuits and hence the name Common collector configuration.

* Input Characteristics.

It is the graph of input current I_B versus input voltage V_{BC} at constant V_{EC}



The common - collector input characteristics are quite different from either common - base or common - emitter input characteristics. The difference is due to the fact that the input voltage V_{BC} is largely determined by the V_{EC} level.

from circuit diagram.

$$V_{EC} = V_{EB} + V_{BC}$$

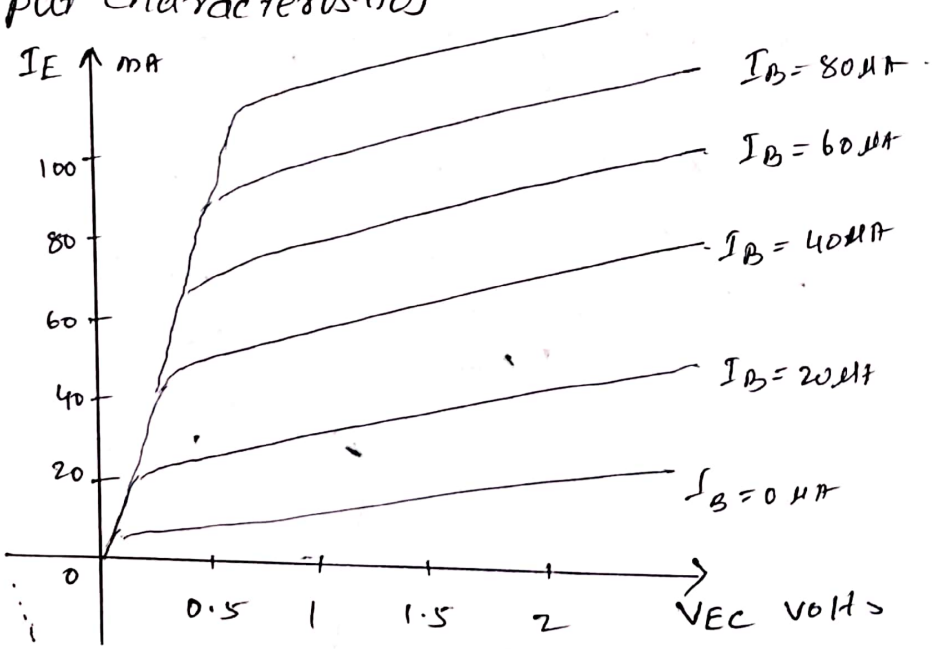
or

$$V_{EB} = V_{EC} - V_{BC}.$$

increasing the level of input voltage V_{BC} with V_{EC} held constant reduces the level of V_{EB} and this reduces I_B.

* output characteristics.

It is the curve between emitter current I_E and collector to emitter voltage V_{EC} at const. base current I_B. Since I_C is approximately equal to I_E, the common-collector output characteristics are practically similar to those of the common-emitter output characteristics



* DC Load line and Bias point.

When transistor used in amplifier circuit, it must be biased in active region (i.e emitter-base junction forward biased and collector-base junction reverse biased) with constant levels of collector, base and emitter current and constant terminal voltages. The levels of I_C and V_{CE} define the transistor dc operating point or quiescent point The circuit that provides this state is known as a bias circuit.

* DC Load line.

The dc load line for a transistor circuit is a straight line drawn on the transistor output characteristics. consider a common emitter npn transistor circuit shown in fig.a) where no signal is applied.

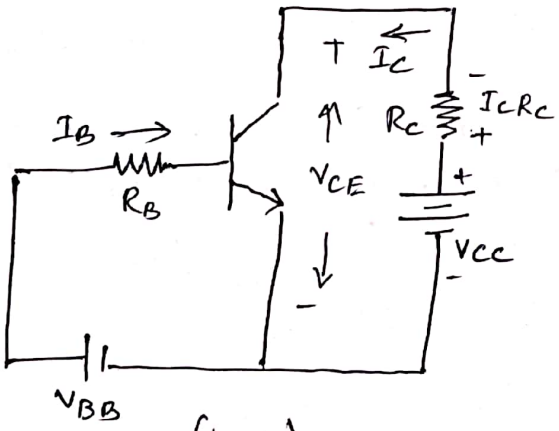


fig.a)

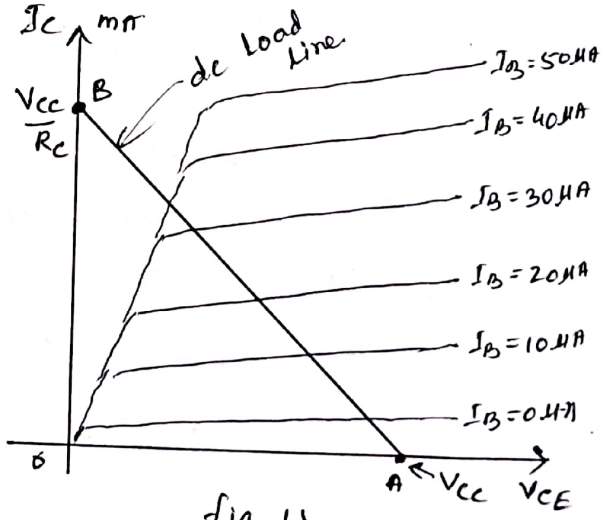


fig.b)

The output characteristics are shown in fig.b).

Applying KVL to output circuit.

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C \quad \text{—1)}$$

As V_{cc} and R_c are fixed values, therefore it is a first degree equation and can be represented by a straight line on the output characteristics.

from eqn 1)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

If we compare, this eqn. with the equation of straigh line $y = mx + c$, where m is the slope of the line and c is the intercept on y-axis. we can draw a straight line on the graph of I_C versus V_{CE} which is having slope $-\frac{1}{R_C}$ and y intercept $\frac{V_{CC}}{R_C}$. To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$

i) when $V_{CE} = V_{CC}$; $I_C = 0$ we get a point A

ii) when $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ we get a point B.

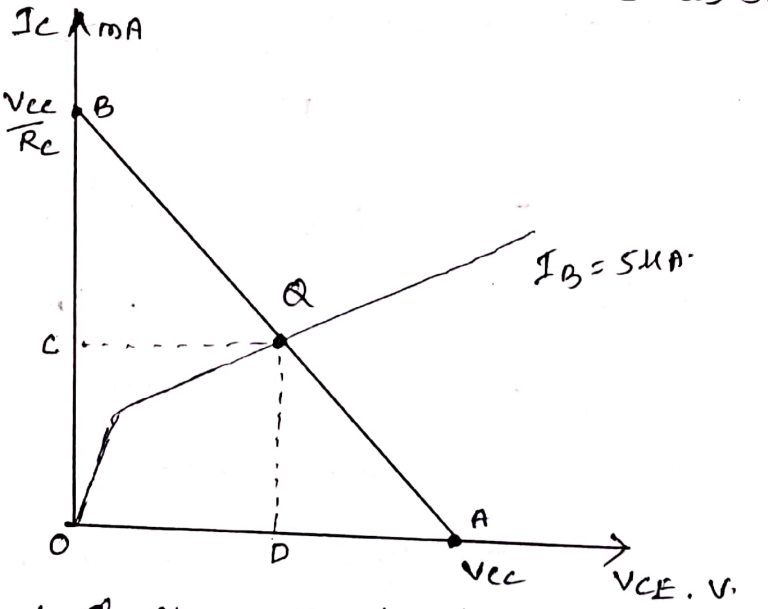
Fig.b) shows the output characteristics of CE conf^n with points A and B, and line drawn between them. The line drawn between points A and B is called dc load line.

So dc load line is a plot of I_C versus V_{CE} for a given value of R_C and a given level of V_{CC}.

* Bias Point (Q-point or operating point).

The dc bias point or quiescent point (Q-point) identifies the transistor collector current and V_{CE} when there is no input signal at the base terminal. It is also called operating point because the variation of I_C and V_{CE} take place about this point when the signal is applied.

Suppose in the absence of input signal, the base current is 5μA. Then I_C and V_{CE} condition in the circuit must be represented by some point on $I_B = 5\mu A$ characteristics. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the dc load line AB as shown in fig.



The point Q where the load line and the characteristics intersect is the only point which satisfies both these conditions. Refer to fig for $I_B = 5\mu A$, the values of I_C and V_{CE} are.

$I_C = OC$ mA

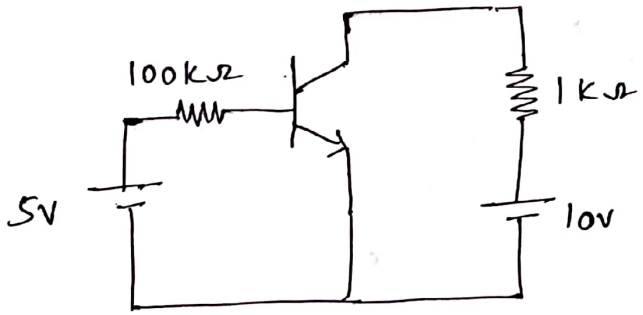
$V_{CE} = OD$ Volts.

Therefore, it follows that the zero signal values of I_C and V_{CE} (operating point or Q-point) are determined by the point where dc load line intersect the proper base current.

* Selection of Q-point.

To get proper amplification without any distortion at the output of the signal, the Q-point has to be selected at the centre of dc load line.

Ex: In the circuit shown in fig, a silicon transistor with $\beta_{dc} = 100$ is used. Find I_C & V_{CE}. Draw the dc load line on output characteristics and indicate the Q-point. assume $V_{BE} = 0.7$ V.



Soln: To determine two points on the load line we assume $V_{CE} = 0$ and $V_{CE} = V_{CC}$.

When $V_{CE} = V_{CC} = 10V$, $I_C = 0mA$ — Pt. A (10V, 0mA)

$V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{10}{1 \times 10^3} = 10mA$ — Pt B (0, 10mA)

To find the Q-point.

Applying KVL on i/p circuit.

$$5 = 100\times10^3 \times I_B + V_{BE}$$

$$I_B = \frac{5 - 0.7}{100\times10^3} = 43\,\mu A.$$

$$I_C = \beta_{dc} \cdot I_B = 100 \times 43\times10^{-6} = 4.3\,mA.$$

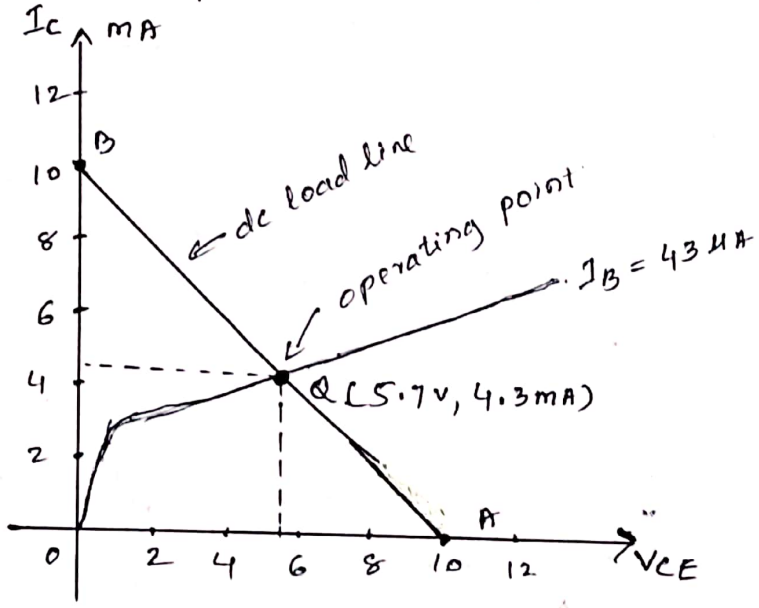
Applying KVL to output circuit.

$$V_{CC} = V_{CE} + I_C R_C.$$

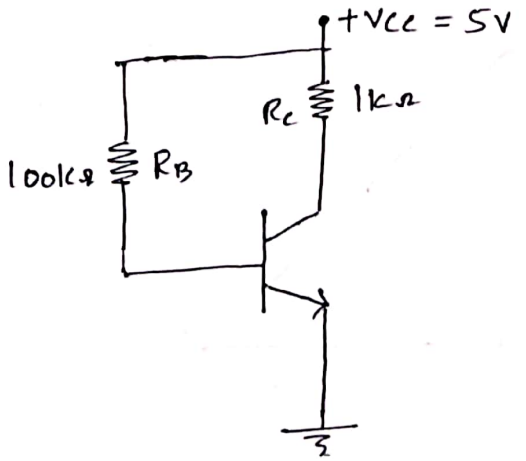
$$\Rightarrow V_{CE} = V_{CC} - I_C R_C = 10 - 4.3\times10^{-3}\times 1\times10^3$$

$$= 5.7\,V.$$

$\therefore$ Q point is (5.7 V, 4.3 mA).



Ex: For the base bias circuit shown in circuit a silicon transistor with $\beta = 50$ is used. draw dc load line and locate the operating point.



Solⁿ: Given $R_B = 100\,k\Omega$, $\beta = 50$, $V_{CC} = 5V$ & $R_C = 1k\Omega$

$V_{BE} = 0.7$ for Si transistor.

Applying KVL to base loop, we have

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{5 - 0.7}{100 \times 10^3}$$

$$= 43\,\mu A$$

$$\therefore I_C = \beta \cdot I_B = 50 \times 43 \times 10^{-6}$$

$$= 2.15 \times 10^{-3} = 2.15\,mA$$

Applying KVL to collector circuit,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_{CC} - I_C R_C = 5 - 2.15 \times 1 \times 10^3$$

$$= 2.85V$$

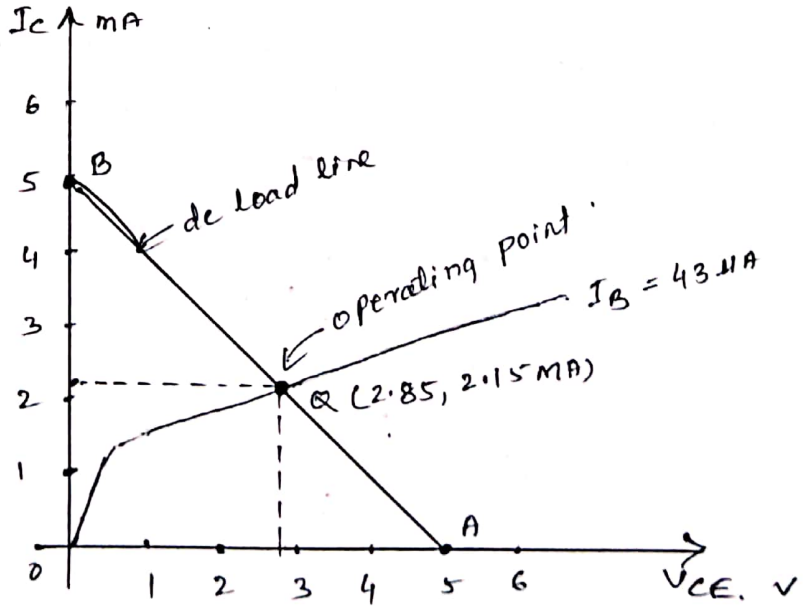
To determine the two points A & B on the load line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$

when $V_{CC} = V_{CC}$, $I_C = 0$ point A (5V, 0mA)

$V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$ pt B (0, 5mA)

$$= \frac{5}{1 \times 10^3} = 5mA$$

dc load line & Q-point.



Module - 2.

* FET

Introduction

FET is unipolar device because, unlike BJT that use both electron and hole current, this operate only with one type of charge carrier. The two main types of FETs are the junction field-effect transistor (JFET) and the Metal oxide semiconductor field-effect transistor (MOSFET). The term field-effect relates to the depletion formed in the channel of a FET as a result of voltage applied on one of its terminals (gate).

Recall that a BJT is a current controlled device, that is, the base current I_B controls the amount of collector current I_C. A FET is different. It is a voltage controlled device. where the voltage between two of the terminals (gate and source) Controls the current through the device. A major advantage of FETs is their very high input resistance. FETs are preferred device in low voltage switching applications because they are faster than BJTs when turned on and off.

* The JFET

The JFET (junction field-effect transistor) is a type of FET that operates with a reverse-biased pn junction to control current in a channel. Depending on the structure, there are two types of JFET, n-channel JFET and p-channel JFET.

* n-channel JFET

- Basic structure

fig. a shows the basic structure of an n-channel JFET. Wire leads are connected to each end of the n-channel; the drain is at upper end, and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel. and both p-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the p-regions. The symbol for n-channel JFET is shown in fig. b.

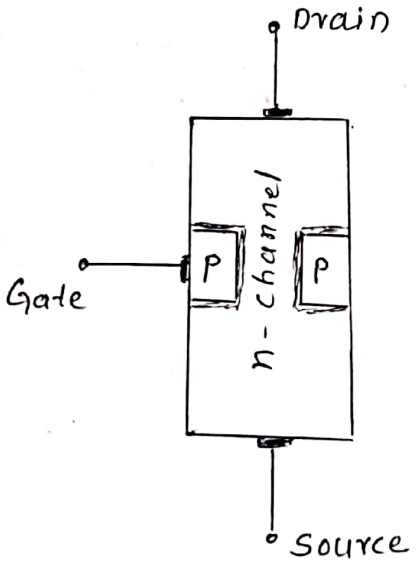


fig. a

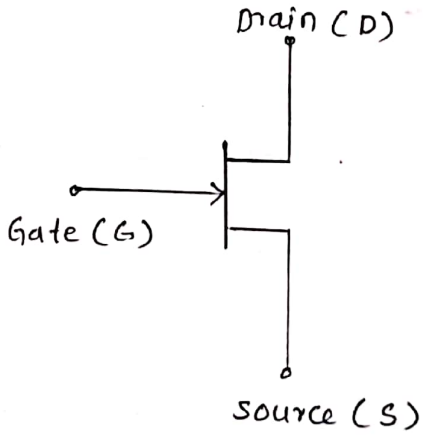
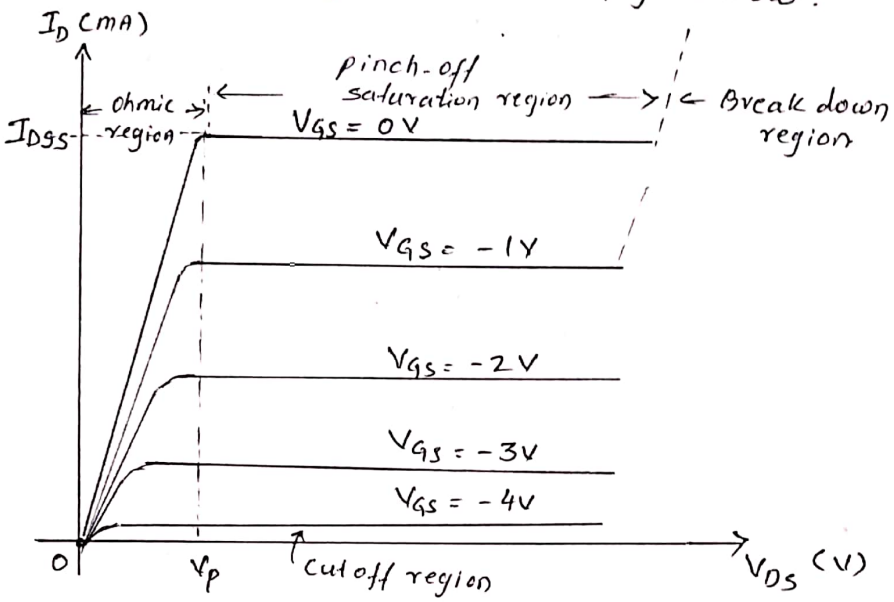


fig b. symbol

Characteristics of N-Channel JFET

1) Drain characteristics: The plot of V_{DS} V/s I_D keeping V_{GS} = constant as shown in fig. below.



The various regions in the drain characteristics are

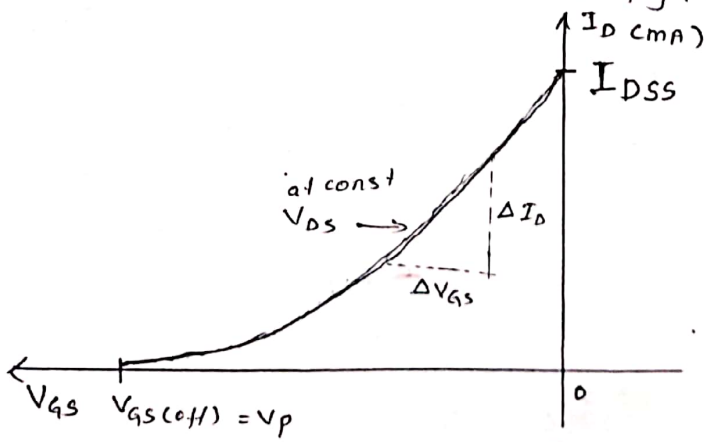
i) Cutoff region: In this region JFET is OFF i.e $I_D = 0$

ii) Ohmic region: In this region the channel of JFET obeys ohm's law

iii) Pinch off/saturation region: This is a region where I_D is maximum for a given V_{GS}, when $V_{GS} = 0V$, $I_D = I_{DSS}$.

iv) Break down region: Breakdown of PN junction takes place and I_D increases abruptly. JFET should not operated in this region.

2) Transfer characteristics: The plot of V_{GS} V/s I_D keeping V_{DS} = constant as shown in fig. below.



3) Square Law Expression for I_D

The transfer characteristics of a JFET can be expressed as,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \quad -- 1)$$

Eqn 1) is the square law expression for I_D

In terms of pinch-off voltage V_p. eqn 1) becomes.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

4) Input resistance: $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$

The JFET data sheet provides the value of I_{GSS} at a certain V_{GS}.

5) Transconductance: $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

from transfer characteristics

Ex: For N-channel JFET, $I_{DSS} = 8mA$; $V_p = -5V$

Determine i) I_D at $V_{GS} = -2$ and $-3V$

ii) V_{GS} at $I_D = 3mA$ & $5mA$.

Soln: We have, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ i) For $V_{GS} = -2V$

$$I_D = 8\left[1 - \frac{(-2)}{(-5)}\right]^2 = 2.88\,mA \quad \text{Ans}$$

For $V_{GS} = -3V$

$$I_D = 8\left[1 - \frac{(-3)}{(-5)}\right]^2 = 1.28\,mA \quad \text{Ans}$$

ii) For $I_D = 3mA$

$$3 = 8\left[1 - \frac{V_{GS}}{(-5)}\right]^2$$

$$\Rightarrow \quad 3 = 8\left[1 + 0.2V_{GS}\right]^2$$

$$\Rightarrow V_{GS} = +1.94V \text{ and } -8.06V$$

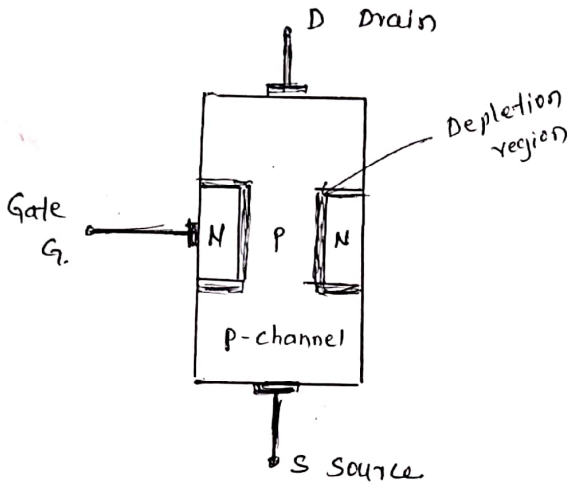
$-8.06V$ neglected as it is greater than V_p

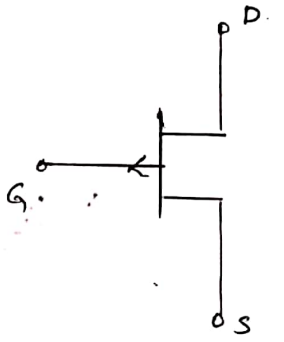
$\therefore V_{GS} = -1.94V$ Ans

for $I_D = 5mA$, $V_{GS} = -1.05V$ Ans

* P-channel JFET

1) Construction. The basic structure of p-channel JFET is shown in fig. below.





Symbol

fig: Basic structure

2) Operation of P-channel JFET

The operation of p-channel JFET is similar to N-channel JFET. In p-channel JFET,

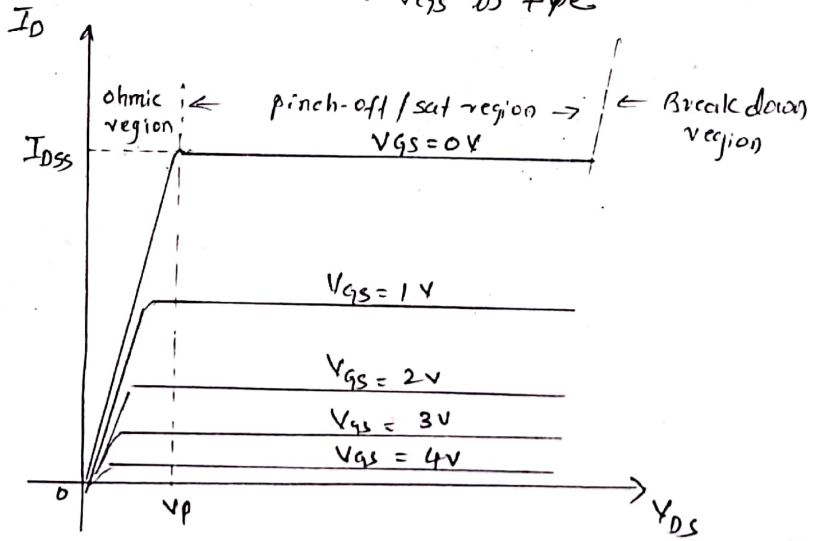
i) V_{GS} is +Ve ii) V_{DS} is -Ve

iii) V_p is +Ve iv) I_D is due to holes.

3) Drain characteristics:

The plot of V_{DS} v/s I_D keeping V_{GS} = constant.

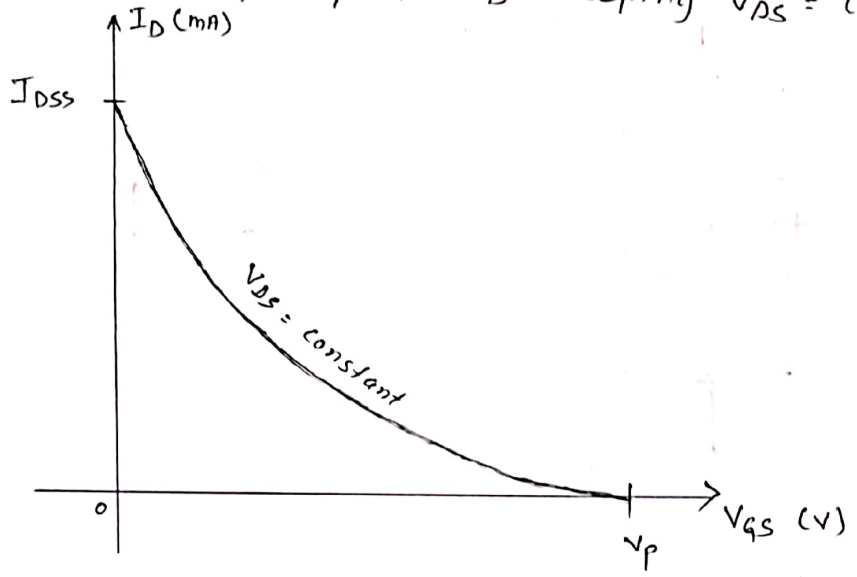
Note V_{DS} is -Ve & V_{GS} is +ve



Drain characteristics.

4) Transfer characteristics.

plot of V_{GS} v/s I_D keeping V_{DS} = Constant.



5) operation of p-channel JFET

when $V_{GS} = 0V$ and $V_{DS} < 0$, the PN junctions are reverse biased. The depletion region width increases with the magnitude of reverse bias i.e as V_{DS} increases the depletion region width increases. Thus the flow of holes from source to drain is restricted to the narrow channel. The width of the channel determines the resistance between drain and source. suppose that V_{DS} is gradually increased from 0V, I_D also increases because the channel behaves as resistance, thus obeys Ohms law. The V_{DS} at which the I_D is maximum i.e I_{DSS} is called pinch off voltage V_p.

Operation of N-channel JFET is same as that of P-channel JFET only. V_{GS} is -ve and V_{DS} is +ve.

* Metal oxide Semiconductor Field Effect Transistor (MOSFET)

The MOSFET is another category of FET. The MOSFET, different from the JFET, has no PN junction structure, instead the Gate of the MOSFET is insulated from the channel by a Silicon dioxide (SiO_2) layer. The two basic types of MOSFET are enhancement (E) and Depletion (D). E-MOSFET and D-MOSFET. E-MOSFET widely used.

- E- MOSFET

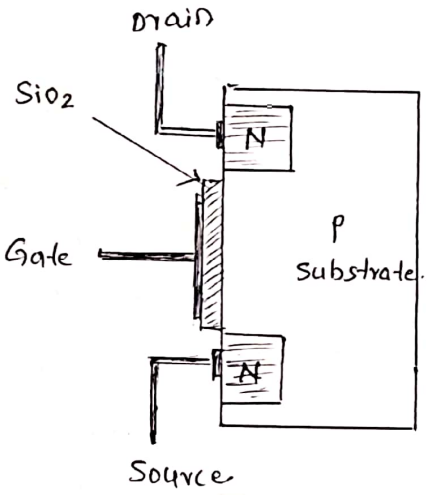


fig1. Basic construction

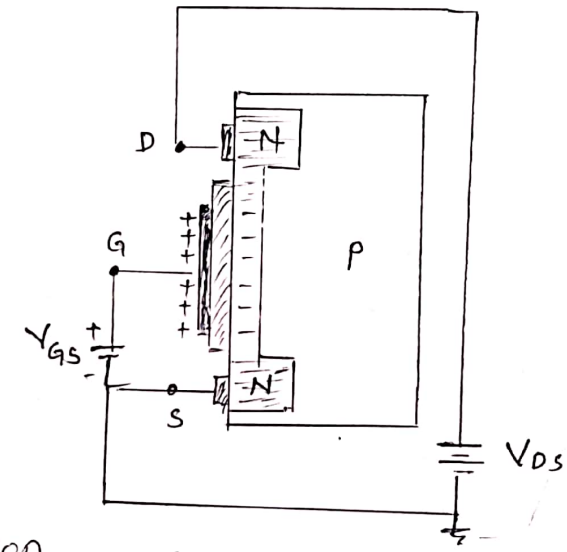
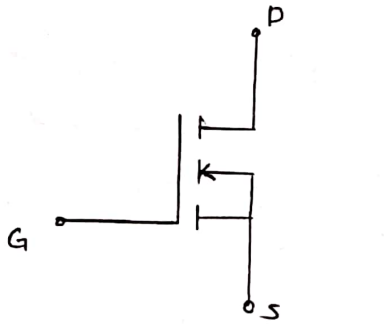
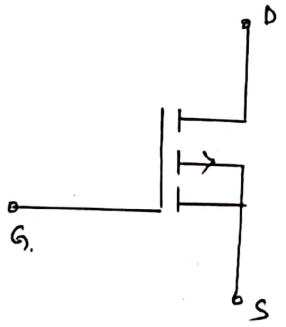


fig2. Induced channel ($V_{GS} > V_{GS(Th)}$)



N-channel MOSFT



p-channel MOSFET

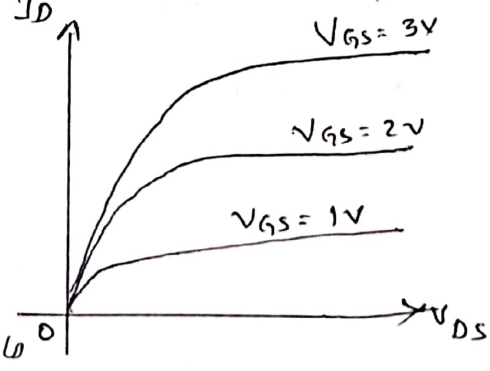
fig3. Symbols

Construction and working

The basic structure of N-channel E-MOSFET is shown in fig.1. A p-type substrate is the basic structure upon which N-type regions are created by diffusion of appropriate impurities. An oxide layer (SiO_2 layer) which acts as an insulator covers entire p-typ substrate and N-type regions. The gate contact is formed on the surface of the oxide layer. The gate is electrically insulated from both N-type regions and p-type substrate.

Consider the +ve voltage applied between gate and source as shown in fig. 2. Because the oxide layer is an insulator sandwiched between conductive regions, a capacitor effect is formed. In this case, the positive voltage at the gate induces negative charges in the p-substrate. This charge results from the minority carriers (electrons) attracted toward the area of the gate. As the number of electrons reaching the region increases, the N-channel is formed gradually and resistance between source and drain decreases. The greater the gate potential (voltage) the lower the channel resistance and higher the drain current I_D. This process is referred as enhancement and resulting device is an enhancement type MOSFET (E-MOSFET).

- Characteristics:



Drain characteristics

V_{DS} v/s I_D at const. V_{GS}.

- Depletion type MOSFET [D-MOSFET]

Another type of MOSFET is the depletion MOSFET (D-MOSFET). Fig.1 illustrates its basic structure of N-channel D-MOSFET.

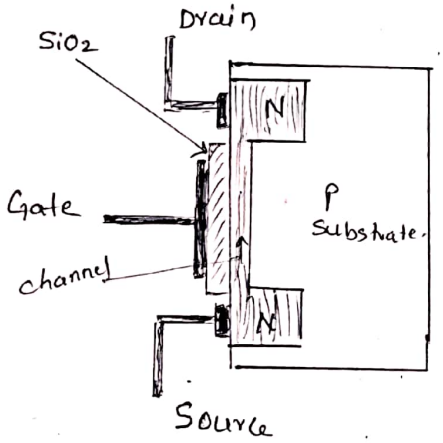


fig.1. Basic structure

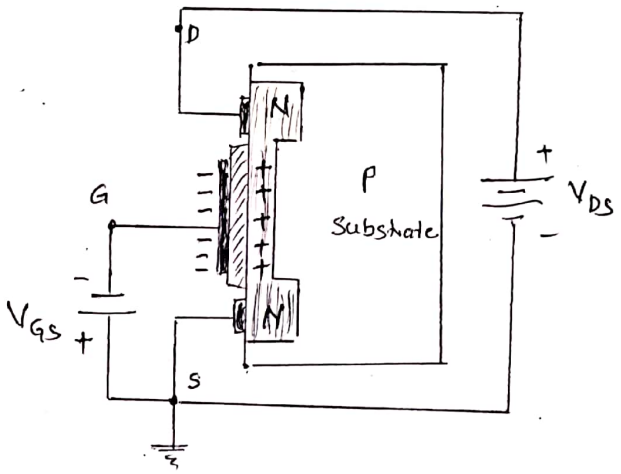


fig 2. Depletion mode: V_{GS} negative

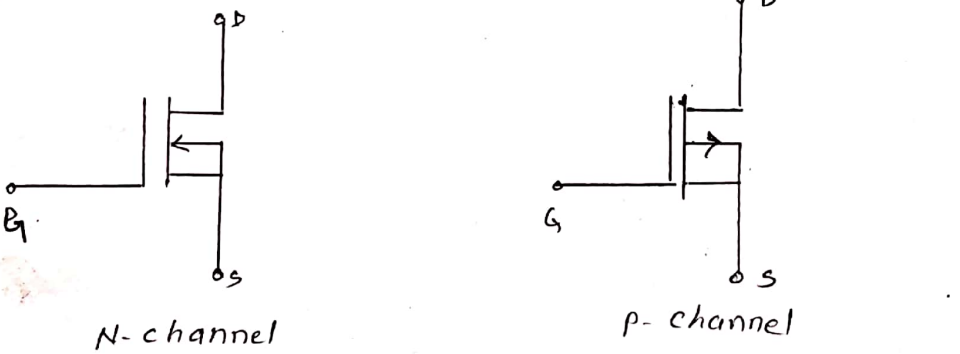


fig 3. Symbols

Basic Construction and Working

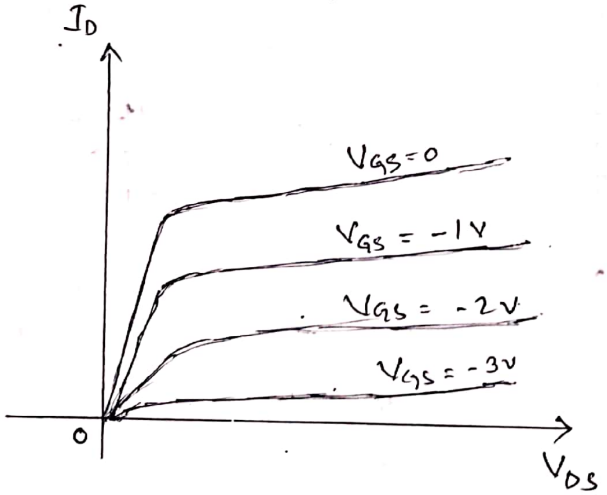
fig 1. shows basic structure of D-MOSFET. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. We will the n-channel device to describe the operation.

The D-MOSFET can operated in either of two modes the depletion mode or enhancement mode. It operates in depletion mode when a negative gate-to-source (-ve V_{GS}) voltage is applied as shown in fig 2.

It will operate in enhancement mode when positive gate-to-source (+ve V_{GS}) voltage is applied. These devices generally operated in depletion mode.

With a negetive gate voltage, the negative charges on the gate repel conduction electrons from the channel leaving positive ions in their place. Thereby, the n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficient negative gate-to-source voltage $V_{GS(off)}$, the channel is totally depleted and the drain current is zero.

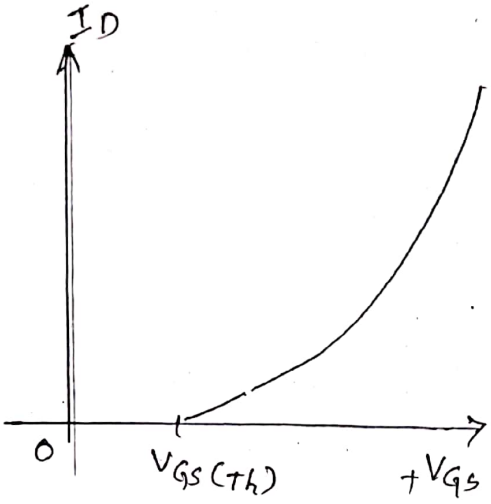
- Characteristics.



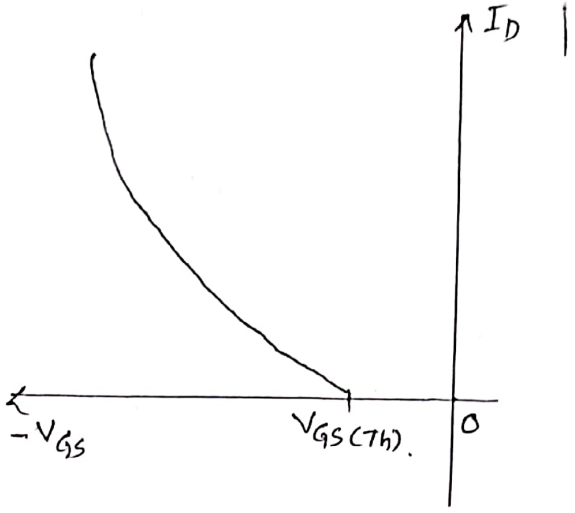
Drain characteristics, V_{DS} v/s I_D at const. V_{GS}

* Transfer characteristics of E-MOSFET

It is a plot of V_{GS} V/s I_D at constant V_{DS}



n-channel E-MOSFET



p-channel E-MOSFET.

Equation for the E-MOSFET transfer characteristic curve is.

$$I_D = K(V_{GS} - V_{GS(TH)})^2$$

The constant K depends on the particular MOSFET and can be determined from the datasheet by taking specified value of I_D, called $I_{D(on)}$ at the given value of V_{GS} and substituting in above eq.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(TH)})^2}$$

Ex: for a E-MOSFET, $I_{D(on)} = 500mA$ at $V_{GS} = 10V$ and $V_{GS(TH)} = 1V$.. Determine the drain current for $V_{GS} = 5V$

Soln: First solve for K,

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(TH)})^2}.$$

$$K = \frac{500 \times 10^{-3}}{(10-1)^2} = 6.17\ mA/V^2.$$

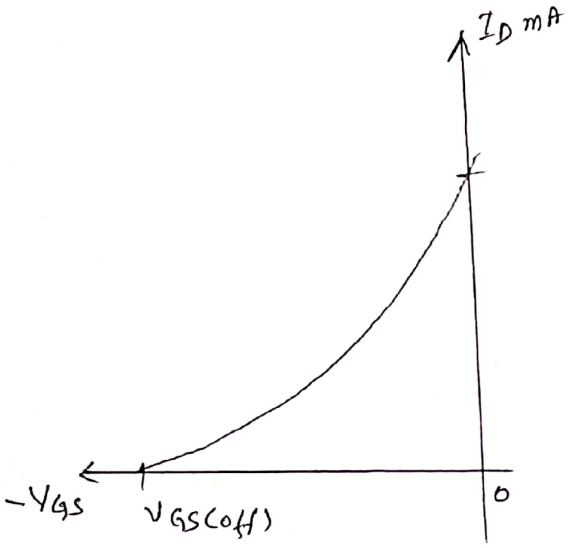
Next using the value of K, calculate I_D for $V_{GS} = 5V$

$$I_D = K(V_{GS} - V_{GS(Th)})^2 = 6.17\ mA/V^2 (5V - 1V)^2 = 98.7\ mA.$$

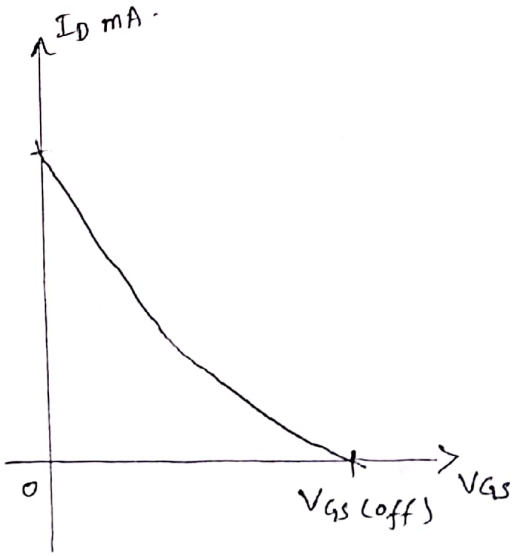
Ex: Repeat the above problem for $I_{D(on)} = 100\ mA$ at $V_{GS} = 8V$ and $V_{GS(Th)} = 4V$. Find I_D when $V_{GS} = 6V$.

* D-MOSFET Transfer characteristics.

It is a plot of V_{GS} V/s I_D



n-channel DMOSFET



p-channel D-MOSFET

The point the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$

As with JFET, $V_{GS(off)} = -V_P$.

The square law expression for the JFET curve also applies to the D-MOSFET curve.

ie $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

Ex: For a certain D-MOSFET, $I_{DSS} = 10mA$ and $V_{GS(off)} = -8V$

a) Is this an n-channel or p-channel.

b) Calculate I_D at $V_{GS} = -3V$

c) Calculate I_D at $V_{GS} = +3V$

Soln: a) The device has a negative $V_{GS(off)}$; therefore, it is an n-channel D-MOSFET.

b) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 10\times10^{-3}\left(1 - \frac{-3}{-8}\right)^2$$

$$= 3.91\ mA.$$

c) $$I_D = 10\times10^{-3}\left(1 - \frac{3}{-8}\right)^2 = 18.9\ mA.$$

QUESTION BANK

Module – 2

Bipolar Junction Transistors

1. With a neat diagram, explain the operation of an *npn* transistor.
2. Explain various currents and voltages flowing through the BJT transistor.
3. Define α and β. Determine the relationship between α and β.
4. A transistor has $\beta = 150$ and I_E is 12 mA. Calculate the approximate collector current (I_C)and base current (I_B).
5. Calculate $_{IC}$ and $_{IE}$ for a transistor that has $_{\alpha dc} = 0.98$ and $_{IB} = 100\ \mu A$. Determine the value of $_{\beta dc}$ (or $_{hFE}$) for the transistor.
6. Calculate α_{dc} and β_{dc} for the transistor if I_C is measured as 1 mA and I_B is 25 μA.
7. Explain BJT current amplification for increasing and decreasing I_B levels.
8. Describe how a transistor can be used as a voltage amplifier.
9. With neat diagram, explain the input and output characteristics of transistor in common base configuration.
10. Explain input and output characteristics of the common emitter configuration.
11. Briefly explain common collector input and output characteristics.
12. With respect to BJT, describe the concept of obtaining the DC load line.
13. Draw the DC load line for transistor and identify Q point.

Field Effect Transistors

1. Explain the construction and operation of N-channel JFET.
2. Make use of N-channel JFET to describe its operation and characteristics.
3. Explain the construction and operation of P-channel JFET.
4. Explain the transfer and drain characteristics of a JFET.
5. Make use of N-channel enhancement type MOSFET and describe the construction and working.
6. Explain the transfer and drain characteristics of enhancement type MOSFET.
7. Explain depletion type MOSFET along with the transfer and drain characteristics.